A Ku Band Converter IC

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Abstract

A Ku-Band VCO converter IC for DBS and CS receivers was developed on a 1.2X2.8mm² chip using a 0.5μm MESFET process. This converter IC includes five(5) functional blocks ; i.e. prescaler, VCO, LNA, mixer and IF Buffer. This converter IC had 7.5dB noise figure and -80dBc/Hz phase noise at a 10KHz offset from a 10.75GHz carrier signal.

I .Introduction

Several X-Ku band DRO converter ICs have been reported for DBS receiver applications. On the other hand, data transmission services have also been started by using communications satellites (CS). The CS system requires a high purity and highly stabilized local signal compared with DBS. A PLL technique has advantages to achieve a high CN ratio at near carrier frequencies.

This paper describes an one chip VCO converter IC which is suitable for a data transmission receiver. The developed IC includes five(5) functional blocks, i.e. prescaler, VCO, low noise amplifier, mixer and IF buffer. The downconverter IC makes it possible to simplify the RF circuits of the CS receivers by only combinning a two-stage HEMT amplifier and IF amplifier. This converter IC achieved a phase noise of -80dBc/Hz at 10KHz offset from a 10.75GHz phase locked carrier. A 0.5μm gate length wafer fabrication process is applicable to both the digital and analog blocks. In section Ⅱ, the circuit design and wafer fabrication process will be discussed, and experimental results will be reported in section Ⅲ. Finally a conclusion will be given in section Ⅳ.

Ⅱ.Design

A block diagram of the converter IC is shown in Figure 1. A division ratio of 12 was selected for the prescaler, in order to separate the prescaler output frequency band from an IF band (950-1750MHz), and also to be able to make a direct connection to a conventional silicon prescaler and PLL IC. In order to minimize the chip area, a lumped constant circuit design approach was used. Circuit designs are described in the following for individual functional blocks. The circuit designs were carried out by using such simulation programs as Super Compact for the LNA block and Spice for the others.

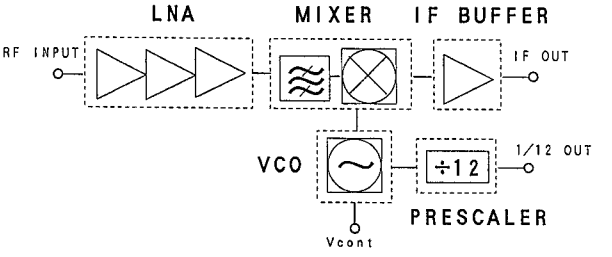

Figure 1. Block Diagram of the Converter IC

LNA and mixer

Figure 2 shows schematic circuits including the LNA, mixer and IF buffer. The LNA is composed of three stages in cascade. A 0.5 X 300μm MESFET is used in each stage.

The single balanced mixer uses an pair of stacked FETs. The single balanced mixer makes it possible to eliminate a IF filter, this effectively reduces the chip area. The LO signals are applied to the second gates and the RF signal is applied to the first gate. Every gate is grounded through large resistors, and the FETs are operating near pinch-off to realize low noise figure.

There are additional circuits around the mixer periphery to improve performance. In order to improve the SSB noise figure, an image rejection filter which consists of inductance and capacitance was adopted at the RF input port. The mixer output is connected to an IF buffer constructed with a source follower. This source follower has an impedance translator function and this operates like a current gain amplifier. A differential LO amplifier was adopted at the LO input port. The output pair from an oscillator were amplified to obtain the sufficient amplitude for the stable mixer operation. A pair of inductances and resistances are used for loads of the LO amplifier, and these inductances create a parallel resonance with the mixer input capacitances.

VCO

A VCO was designed based on an astable multivibrator circuit which had a complementary output pair. This output pair can be directly used for complementary clocks of prescaler input, and is also suitable for the balanced mixer.

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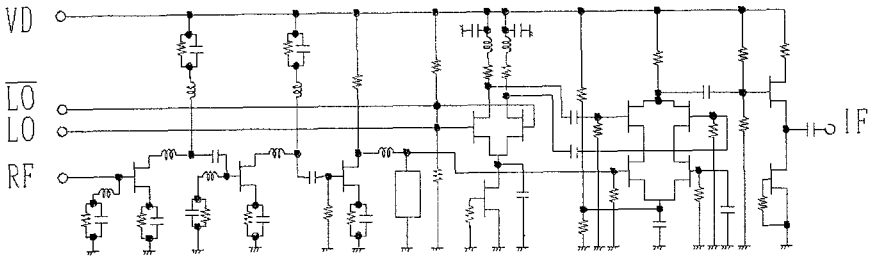

Figure 2. Circuit Diagram of the LNA, mixer and IF buffer

Figure 3 shows a schematic circuit of the VCO. The VCO circuit is composed of a pair of oscillating FETs, resonant circuits, varactors and output buffers, constructed with a source follower circuit. The resonant circuits and the varactors determine the oscillation frequency depending on an applied varactor voltage. The gate width was designed to be 50um, 85um, and 170um, for the oscillating FET, operating FET and current source FET of the source follower respectively. The resonant circuit was designed by using such lumped elements as spiral inductors and interdigital capacitors to minimize the deviation of the oscillation frequency against wafer fabrication deviations. The varactors were schottky gate of fundamental FETs, whose gate length and width were designed to be 0.8um and 100um, respectively. Three varactors were connected in series to reduce capacitances of these varactors, and also to reduce the modulation sensitivity of the VCO. This is because high modulation sensitivity causes the PLL operation to be unstable.

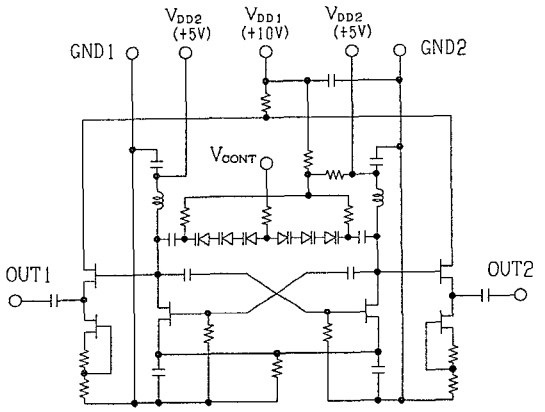

Figure 3. Circuit Diagram of the VCO

Prescaler

The prescaler is one of the key blocks in this converter IC.

In order to obtain a division ratio of 12, there are some combinations of such basic blocks as 1/2 and 1/3. The practical combinations are 1/2-1/3-1/2 and 1/2-1/2-1/3. The former combination has some difficulty to realize a 1/3 block due to the high operating frequency requirement of 6GHz. On the other hand, the later combination is easier than the former. However the later one has such a fatal disadvantage that it's duty cycle of the divided output signal becomes 1:2 instead of 1:1(50%) due to the 1/3 operation of the last stage. This means that the capability of direct connection to a conventional silicon prescaler and PLL IC becomes difficult. Therefore the former combination was attempted, and a 1/3 operation was simulated over 7GHz with a dynamic prescaler.

The divide-by-12 prescaler which was composed of cascaded 1/2-1/3-1/2 dynamic prescaler sub-blocks is shown in Figure 4. Each prescaler subblock includes an inverter, buffer amplifier, and NOR (only 1/3 subblock) circuit, which are constructed of BFL (Buffered FET Logic) circuits. Gate widths were designed to be 40um, 30um and 10um for the BFL circuits of the 1/2, 1/3 and final 1/2 subblocks, and also 20um, 20um and 6um for the transfer gate FETs, respectively.

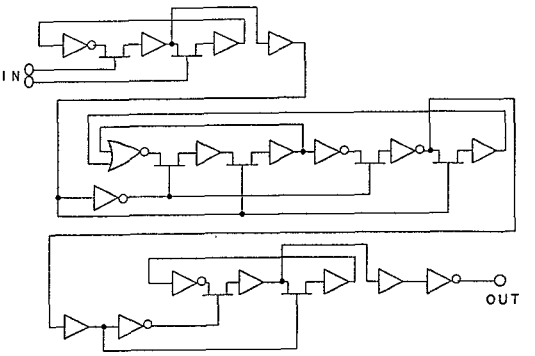

Figure 4. Block Diagram of the Divide-by-12 Prescaler

In this work, we also tried another newly developed technique to decrease total current consumption of the divide-by-12 prescaler. It is the so-called stacked configuration. Figure 5 shows the principle of operation of this configuration. In the first stage of development, the DC power was applied (+5V) to each subblocks and total current consumption was more than 80mA. In the DBS and CS application +15V DC power is supplied from an indoor unit. Therefore, from a power consumption point of view, it was advantageous to decrease the current even if the applied voltage is stepped up.

By using the stacked configuration, it can be expected to decrease the total current consumption of the prescaler by a half.

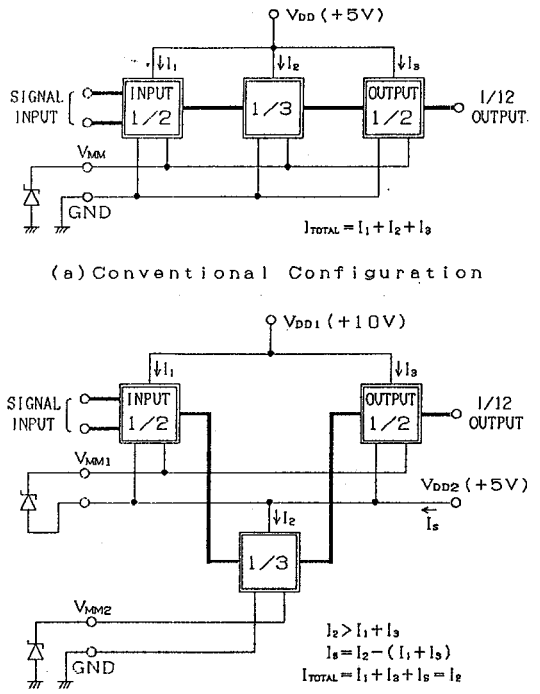

Figure 5. Principle of the Stacked Configuration of Divide-by-12 Prescaler

Wafer fabrication

The fundamental FETs used in this IC have T-shaped WSi offset gates with TiN/Pt/Au on the top of the WSi for reducing the gate resistance. The gate lengths are 0.5μm. Si+ion-implantation was used to form active layers for FETs, diodes and resistors. The FET Vt was chosen to be about -1.0V. The chip size is 1.2 X 2.8mm^2, and a chip photograph is shown in Figure 6.

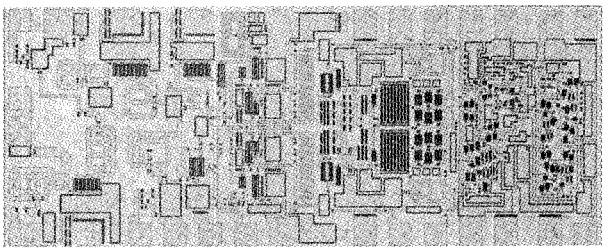

Figure 6. Photograph of the Converter IC (chip size : 1.2 X2.8mm^2)

Ⅲ.Experimental Results

Mixer

The measured conversion gain and noise figure of the IC are shown in Figure 7. A noise figure of less than 8dB and a conversion gain of more than 10dB have been achived for 11.7~12.5GHz.

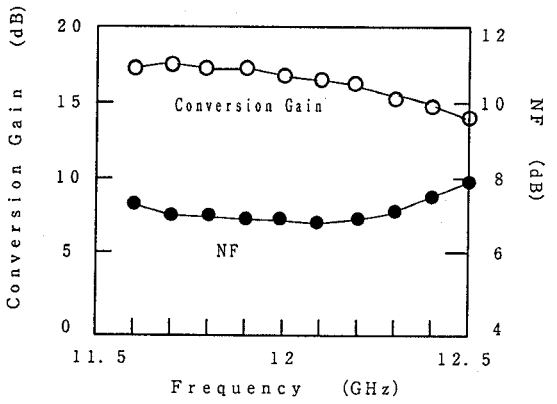

Figure 7. Conversion Gain and NF of the Converter IC

VCO

Figure 8 shows the frequency vs. voltage characteristic of the VCO. The ocsillation frequency range was from 10.4 to 11.1GHz and the maximum modulation sensitivity was about 150MHz/V under 0~+8V external control voltage. This X-band operation using an astable multivibrator circuit is the first report at a practical level.

Prescaler

Figure 9 shows the input sensitivity characteristic of a divide-by-12 prescaler block with a 50 Ω load. In the converter IC, input power to the prescaler from the VCO was estimated at about -3dBm, so the operating frequency range of the prescaler could be also estimated to be from 9GHz to 12GHz. This frequency range has enough margin to operate at 10.75GHz frequency. Therefore a high process yield can be expected. In addition, the prescaler output power was more than -7dBm from 800MHz to 1000MHz under a 50 Ω loaded condition. This power is enogh to drive a conventional silicon prescaler and PLL IC. The reduction of current consumption was achieved by using the stacked configuration, the measured current was 46% lower than the un-stacked prescaler.

Moreover, the 1/3 dynamic prescaler was operated up to 7GHz which is the first report. This result indicates an advance of dynamic prescaler technology.

PLO (Phase Locked Oscllator)

To confirm the PLL operation of this converter IC, the VCO and the prescaler blocks were evaluated with a PLL breadboard. Figure 10 shows a block diagram of this measurement system. The reference frequency for the TTL phase frequency detector IC was chosen to be 7MHz, then the phase locked frequency of the VCO was set to 10.75GHz. The loop bandwidth of the PLL was set to 300KHz. Figure 11 shows an observed output spectrum of the phase locked VCO. The phase noise was -80dBc/Hz at 10KHz offset frequency from a 10.75GHz carrier.

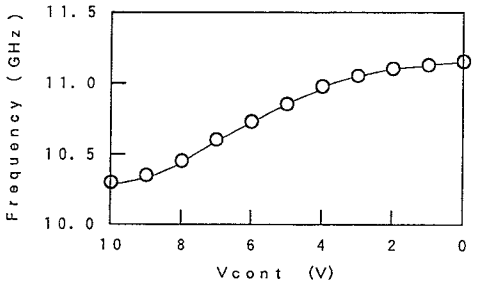

Figure 8. Voltage-Frequency Characteristic of the VCO

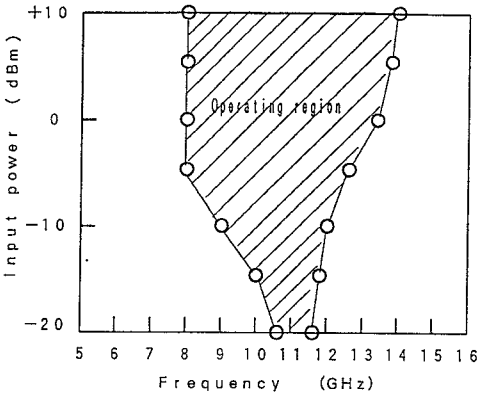

Figure 9. Operating region of the Prescaler

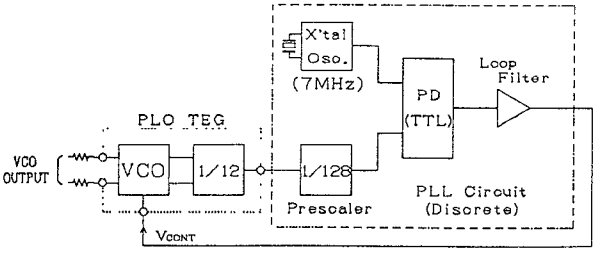

Figure 10. Block Diagram of the PLO Evaluation System

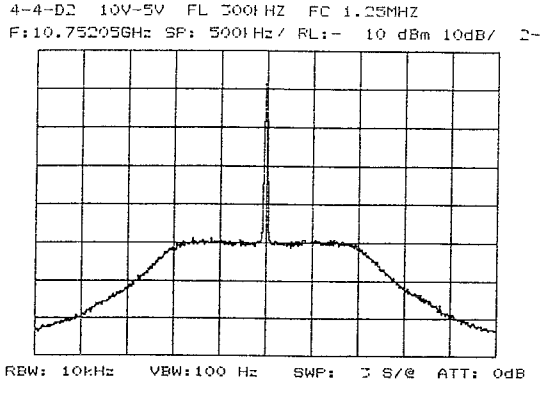

Figure 11. Output Spectrum of the Phase Locked VCO

The overall performance is shown in the following table.

SPECIFICATION	MEASURED VALUE	CONDITION
RF band	11.7~12.5GHz	LO. 10.75GHz
SSB Noise Fiqure.	8.0dB	
Conversion Gain	10dB	
Phase Noise	80dBc/Hz	with PLL circuit at 10KHz offset.
Sensitivity of VCO	150MHz/V	
Frequency range of VCO	10.4~11.1GHz	0~8V control voltage range.
Output Power of Prescaler	-7dBm	terminated with 50OHM.
Operating range of Prescaler	9~12GHz	
Current Consumption	97mA/10V 43mA/5V	

Ⅳ.Conclusion

An one-chip downconverter IC composed of prescaler, VCO, LNA, mixer, and IF Buffer, has been developed for DBS and CS applications. This IC was fablicated on a 1.2 X 2.8㎟ chip. The noise figure was less than 8dB and the conversion gain was more than 10dB and the observed phase noise was -80dBc/Hz at a 10KHz offset frequency from a 10.75GHz carrier. This performance can meet the CS receiver requirements. This is the first report of the dynamic 1/12 prescaler operating in the 9 to 12GHz range, and a multivibrator operating at X-Band in a multi-function IC. These succesful results made it possible to realize the one chip VCO downconverter IC, and to directly connect to a conventional silicon prescaler and PLL IC. This IC is promising for miniaturization and cost reduction of CS recievers.

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